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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/867,137	05/29/2001	Joseph J. Ervin	P6451	7466

21127 7590 03/25/2004

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	2

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,137	ERVIN, JOSEPH J.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. An incorporated reference of Application 09/630,099 is on page 7. Applicant should update the incorporated reference's status.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "tree hierarchy" in claims 4 and 6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 11 recite that "*small enough* to avoid rise time problem". The claim language is ambiguous; it fails to particularly point out and distinctly claim the invention. Claims 2-10 and 12-20 are rejected because they incorporate the parent claim's limitations.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-7 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte (6,092,138) in view of Jennings et al. (U.S. Patent No. 5,632,021.

Referring to claim 1: Schutte discloses a bridged segmented I2C bus system connecting master devices and slave devices (figure 1), and since the I2C specification requires the rise-time specification of one microsecond, thus, Schutte's I2C bus system is constructed in considering of this rise time requirement. Thus, it discloses the claimed limitations (a) and (c).

Schutte discloses connecting the I2C with a bridge, but Schutte does not explicitly disclose selectively forward transactions. Jennings discloses a cascaded/tree bus bridge system connecting different bus segments (figure 3, structures 311, PCI bus 0 and 1) with bus bridges (figure 3, structures 315, 331 and 332). Jennings discloses that each bridge's memory base register defines the base address for determining when to forward memory transactions (column 7, lines 16-18); thus Jennings selectively forwards transactions and commands from one bus segment to another, which is the claimed limitation (b). Jennings further discloses connecting master devices and slave devices to the bus segments (figure 3, abstract), which is the claimed limitation (c).

Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Jennings' teaching onto Schutte at the time Applicant made the invention because Jennings teaches one to expand the capacity of a bus system.

Referring to claim 2: Jennings discloses a memory mapping (figure 6, column 7, lines 44-45) within the bridge, which is the claimed address bitmap.

Referring to claim 3: Jennings discloses a based register and a limit register (column 7, lines 15-28), which are the claimed pair of range registers.

Referring to claim 4: Jennings discloses a tree hierarchy (figure 3).

Referring to claim 5: Jennings discloses that the bridge's registers have no default values and must be initialized (column 7, lines 18-20), and these registers include base register, limit register, and registers for address mapping (figure 6, column 7, lines 38-55). Jennings discloses that configuration software will initialize the registers' values (column 7, lines 19-20). The

configuration software is the claimed programming means, and the processor executing the software is the claimed bus master.

Referring to claim 6: Jennings discloses a bus master at the root level (figure 3, structure 310, the CPU).

Referring to claim 7: Schutte discloses a bi-directional bridge (figure 1, structure 14).

Referring to claim 11: Schutte discloses a bridged segmented I2C bus system connecting master devices and slave devices (figure 1), and as the Applicant states that the I2C specification requires the rise-time specification of one microsecond, thus, Schutte's I2C bus system will be constructed in considering of this rise time requirement.

Schutte discloses connecting the I2C with a bridge, but Schutte does not explicitly disclose selectively forward transactions. Jennings discloses a cascaded/tree bus bridge system connecting different bus segments (figure 3, structures 311, PCI bus 0 and 1) with bus bridges (figure 3, structures 315, 331 and 332). Jennings discloses that each bridge's memory base register defines the base address for determining when to forward memory transactions (column 7, lines 16-18); thus Jennings selectively forwards transactions and commands from one bus segment to another. Jennings further discloses connecting master devices and slave devices to the bus segments (figure 3, abstract).

Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Jennings' teaching onto Schutte at the time Applicant made the invention because Jennings teaches one to expand the capacity of a bus system.

Referring to claim 12: Jennings discloses a memory mapping (figure 6, column 7, lines 44-45) within the bridge, which is the claimed address bitmap.

Referring to claim 13: Jennings discloses a based register and a limit register (column 7, lines 15-28), which are the claimed pair of range registers.

Referring to claim 14: Jennings discloses a tree hierarchy (figure 3).

Referring to claim 15: Jennings discloses that the bridge's registers have no default values and must be initialized (column 7, lines 18-20), and these registers include base register, limit register, and registers for address mapping (figure 6, column 7, lines 38-55). Jennings discloses that configuration software will initialize the registers' values (column 7, lines 19-20). The CPU that executes the configuration software is the claimed configuration host.

Referring to claim 16: Jennings discloses a bus master at the root level (figure 3, structure 310, the CPU).

Referring to claim 17: Schutte discloses a bi-directional bridge (figure 1, structure 14).

6. Claims 8-9 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte in view of Jennings as applied to claims 1-7 and 11-17, further in view of Bell et al. (U.S. Patent No. 5,546,546).

Referring to claims 8-9 and 18-19: Jennings discloses two unidirectional bridges (figure 3, structures 331 and 332) to connect two bus segments (figure 3, structures buses 0 and 1). Neither Schuttle nor Jennings explicitly discloses a bridge ID. Bell discloses a bridging system for maintaining transaction order, which each bridge includes an address mapping logic and a bridge ID (column 8, lines 6). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adopt the teaching of Bell and

Jennings onto Schuttle because Jennings teaches one to expand the capacity of a bridged bus system and Bell teaches one to maintain the transaction order in a bridged system.

7. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte in view of Jennings, and in further view of Pettey et al. (U.S. Patent No. 6,594,712).

Referring to claims 10 and 20: Schutte and Jennings' disclosures are stated above; furthermore, Jennings discloses each bridge's address mapping, which discloses that each command/transaction includes a designated address/slave device address. Jennings further discloses that the bridge has a buffer for storing each transaction's data (column 3, lines 9-11). Thus, Jennings discloses each command includes both data and slave device address. Neither Schutte nor Jennings explicitly discloses that at least two slave devices have the same address.

In addition to Applicant's specification statement that it is anticipated that an InfiniBandsM with Target Channel Adapter (TCA) will have the slave devices with same addresses (Specification, page 11), Pettey discloses an InfiniBandsM system with TCA. Pettey discloses that it is known to apply the RAID (column 1, lines 66-67) on top of the system, which the RAID will have at least two slave devices with the same address. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adopt the teachings of Jennings and Pettey onto Schutte because Jennings teaches one to expand the capacity of a bus system and Pettey teaches one to avoid the reduction in usable bandwidth of the local bus and of a system memory by not double-buffering the data and transferring the data directly from the I/O controller to the channel adapter (column 3, lines 21-24).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin King
March 19, 2004

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